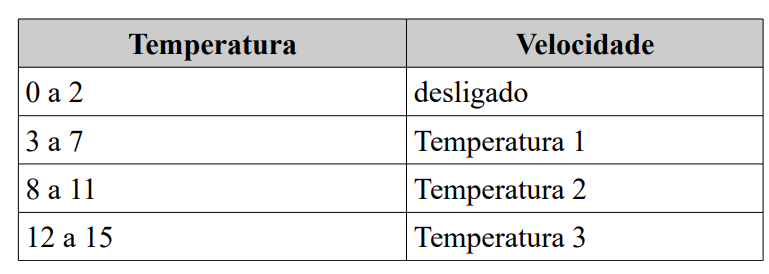
**Alunos**: Felipe Braz Marques, Mariana Macedo Santos, Matheus Peixoto Ribeiro Vieira, Nicolas Expedito Lana Mendes, Pedro Henrique Rabelo Leão de Oliveira, Vinicius Nunes dos Anjos

**Disciplina**: BCC 265



A saída terá dois bits:

Desligado: 00

Temperatura 1: 01

Temperatura 2: 10

Temperatura 3: 11

|  | **Entradas** | | | | **Saídas** | | **Saída em decimal** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **S1** | **S2** |
| **0** | 0 | 0 | 0 | 0 | 0 | 0 | **0** |
| **1** | 0 | 0 | 0 | 1 | 0 | 0 |
| **2** | 0 | 0 | 1 | 0 | 0 | 0 |
| **3** | 0 | 0 | 1 | 1 | 0 | 1 | **1** |
| **4** | 0 | 1 | 0 | 0 | 0 | 1 |
| **5** | 0 | 1 | 0 | 1 | 0 | 1 |
| **6** | 0 | 1 | 1 | 0 | 0 | 1 |
| **7** | 0 | 1 | 1 | 1 | 0 | 1 |
| **8** | 1 | 0 | 0 | 0 | 1 | 0 | **2** |
| **9** | 1 | 0 | 0 | 1 | 1 | 0 |
| **10** | 1 | 0 | 1 | 0 | 1 | 0 |
| **11** | 1 | 0 | 1 | 1 | 1 | 0 |
| **12** | 1 | 1 | 0 | 0 | 1 | 1 | **3** |
| **13** | 1 | 1 | 0 | 1 | 1 | 1 |
| **14** | 1 | 1 | 1 | 0 | 1 | 1 |
| **15** | 1 | 1 | 1 | 1 | 1 | 1 |

Mapa saída S1:

| X | ~A~B | ~AB | AB | A~B |
| --- | --- | --- | --- | --- |
| ~C~D |  |  | 1 | 1 |
| ~CD |  |  | 1 | 1 |
| CD |  |  | 1 | 1 |
| C~D |  |  | 1 | 1 |

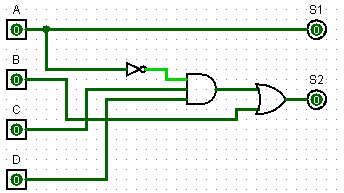
Equação para S1: A

Mapa saída S2:

| X | ~A~B | ~AB | AB | A~B |
| --- | --- | --- | --- | --- |
| ~C~D |  | 1 | 1 |  |
| ~CD |  | 1 | 1 |  |
| CD | 1 | 1 | 1 |  |
| C~D |  | 1 | 1 |  |

Equação para S2: ~ACD + B

Mapa de circuitos:



**Sistema em verilog:**

module ventilador(a,b,c,d,s1,s2);

input a,b,c,d;

output s1, s2;

assign s1 = a;

assign s2 = (~a&c&d) | b;

endmodule

module simulador;

reg a,b,c,d;

wire s1, s2;

initial

begin

a = 0;

b = 0;

c = 0;

d = 0;

end

always

begin

#1 {a, b, c, d} = {a, b, c, d} + 1;

end

initial

begin

#15 $finish;

end

initial

begin

$display("tempo\t A\t B\t C\t D\t S1\t S2\t");

$monitor("%5d\t %b\t %b\t %b\t %b\t %b\t %b\t", $time, a, b, c, d, s1, s2);

end

ventilador sim(.a(a), .b(b), .c(c), .d(d), .s1(s1), .s2(s2));

endmodule

Circuito no Proteus:

